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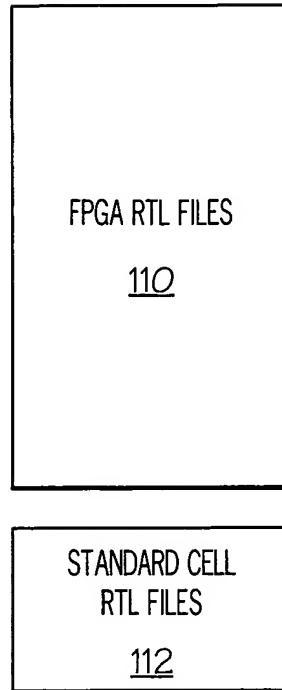


FIG. 1A  
(PRIOR ART)

100 ↘

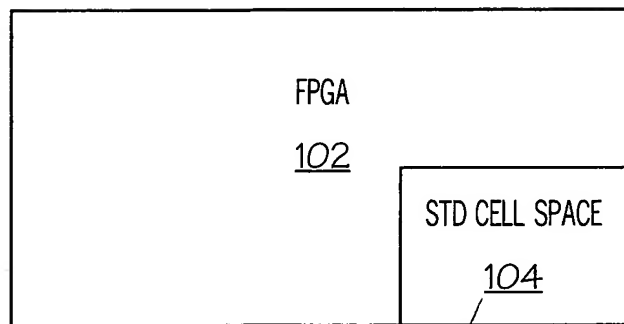


FIG. 1B

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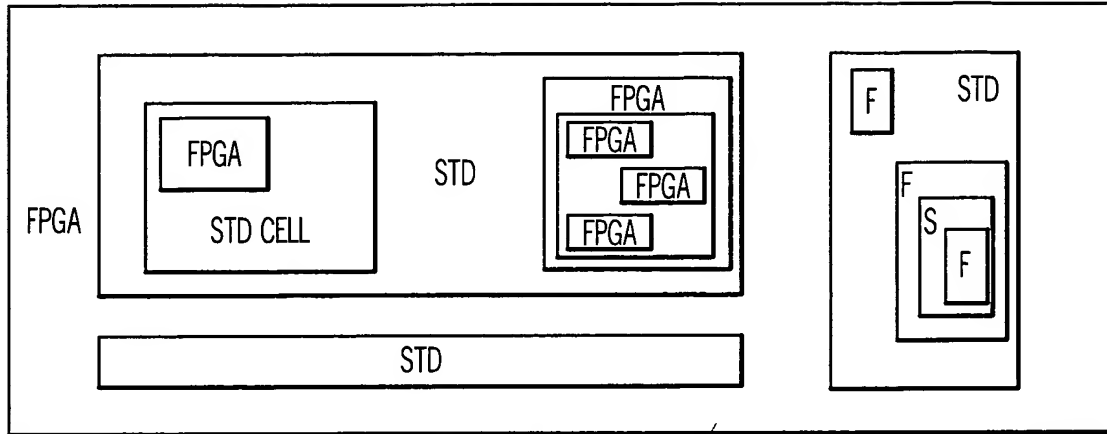


FIG. 1C

200

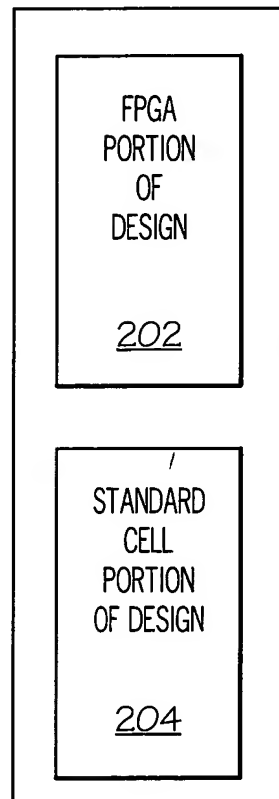
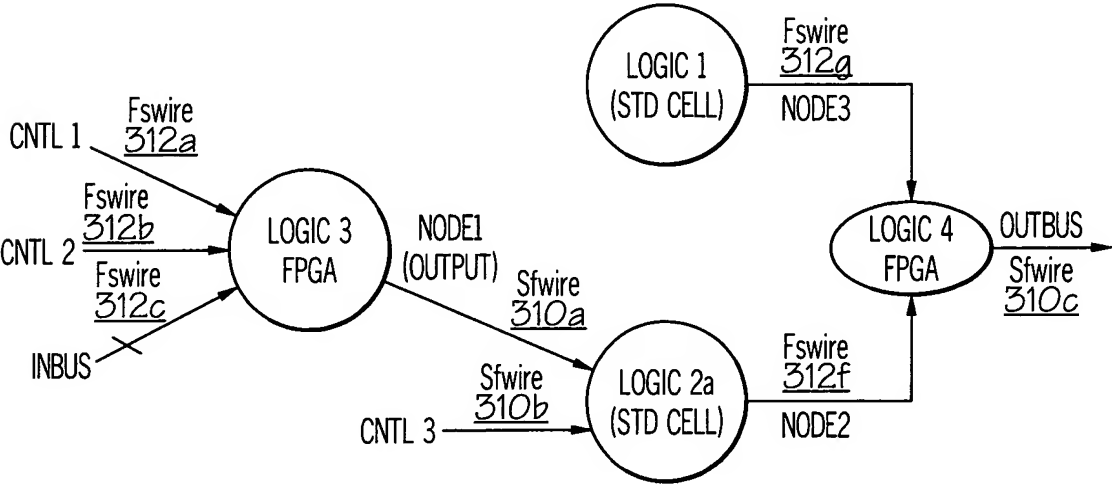


FIG. 2

	WIRE TYPE	MEANING	FIXED OR ADJUSTABLE
302~	(S)wire	STANDARD CEL	FIXED
304~	Fwire	FPGA	FIXED
306~	sFwire	TOOL REPARTITION REQUEST: FPGA -> STD CELL	ADJUSTABLE
308~	fSwire	TOOL REPARTITION REQUEST: STD CELL -> FPGA	ADJUSTABLE
310~	Sfwire	STANDARD CELL, ACCEPTED BY DESIGNER	ADJUSTABLE
312~	Ffwire	FPGA, ACCEPTED BY DESIGNER	ADJUSTABLE

FIG. 3 ✓

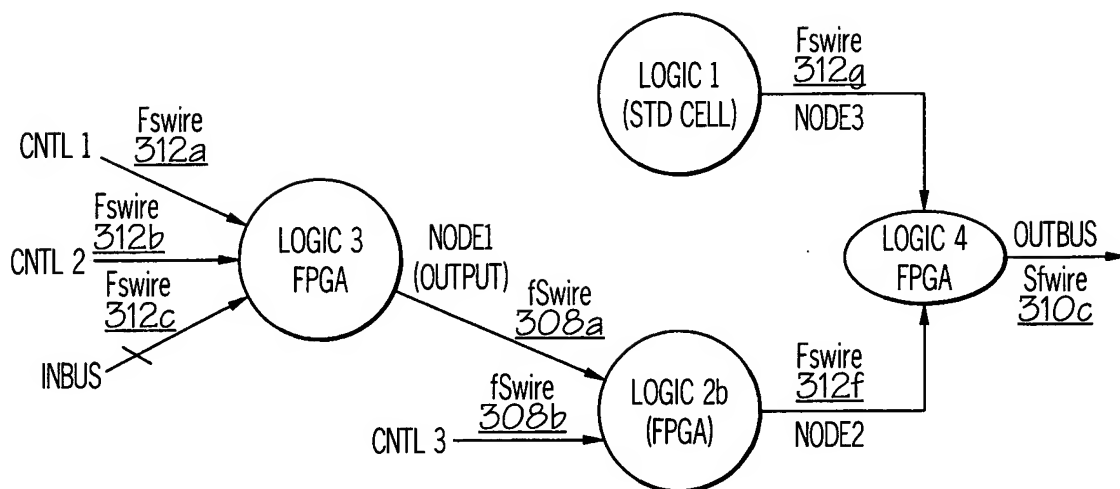


EXAMPLE VERILOG

```
module MyDesign (CNTL1, CNTL2, INBUS, CNTL3,
OUTBUS);
input Fswire CNTL1, CNTL2;
input Fswire [7:0] INBUS;
input Fswire CNTL3;
Sfwire NODE1;
Fswire NODE2, NODE3;
output Sfwire [7:0] OUTBUS;
```

FIG. 4A ✓

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EXAMPLE VERILOG

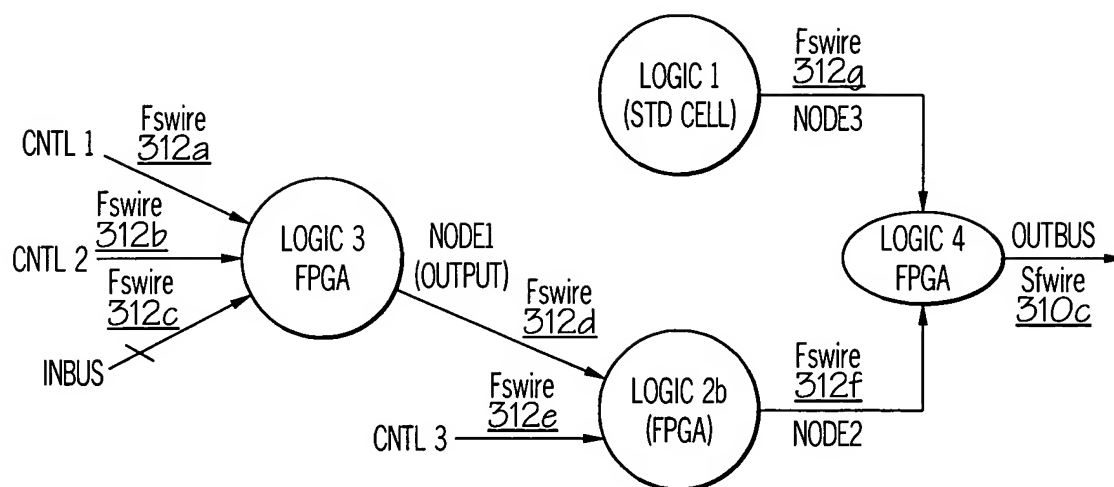
```

module MyDesign (CNTL1, CNTL2, INBUS, CNTL3,
OUTBUS);
input Fswire CNTL1, CNTL2;
input Fswire [7:0] INBUS;
input Fswire CNTL3;
fSwire NODE1;
Fswire NODE2, NODE3;
ouput Sfwire [7:0] OUTBUS;

```

FIG. 4B ✓

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EXAMPLE VERILOG

```

module MyDesign (CNTL1, CNTL2, INBUS, CNTL3,
OUTBUS);
input Fswire CNTL1, CNTL2;
input Fswire [7:0] INBUS;
input Fswire CNTL3;
Fswire NODE1;
Fswire NODE2, NODE3;
output Sfwire [7:0] OUTBUS;
  
```

FIG. 4C

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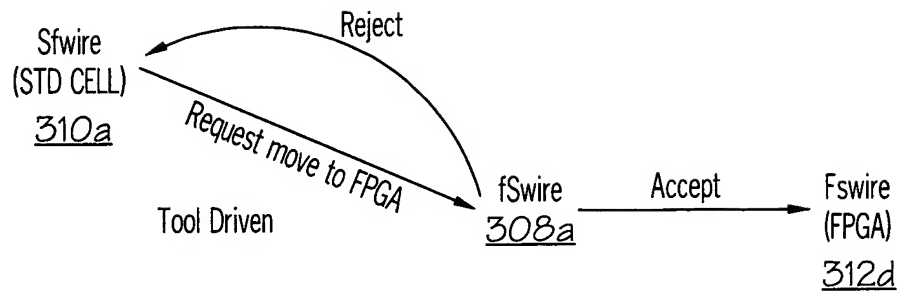


FIG. 5A

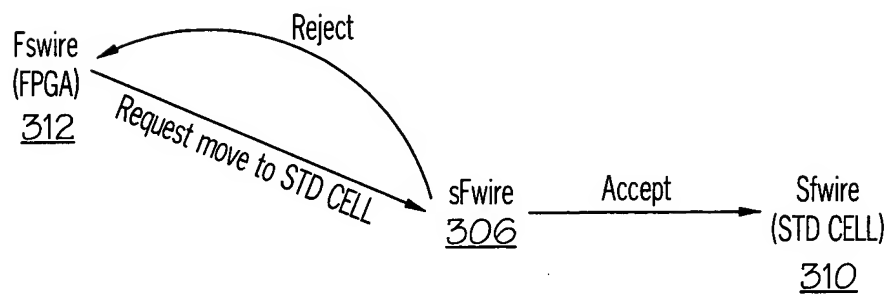


FIG. 5B

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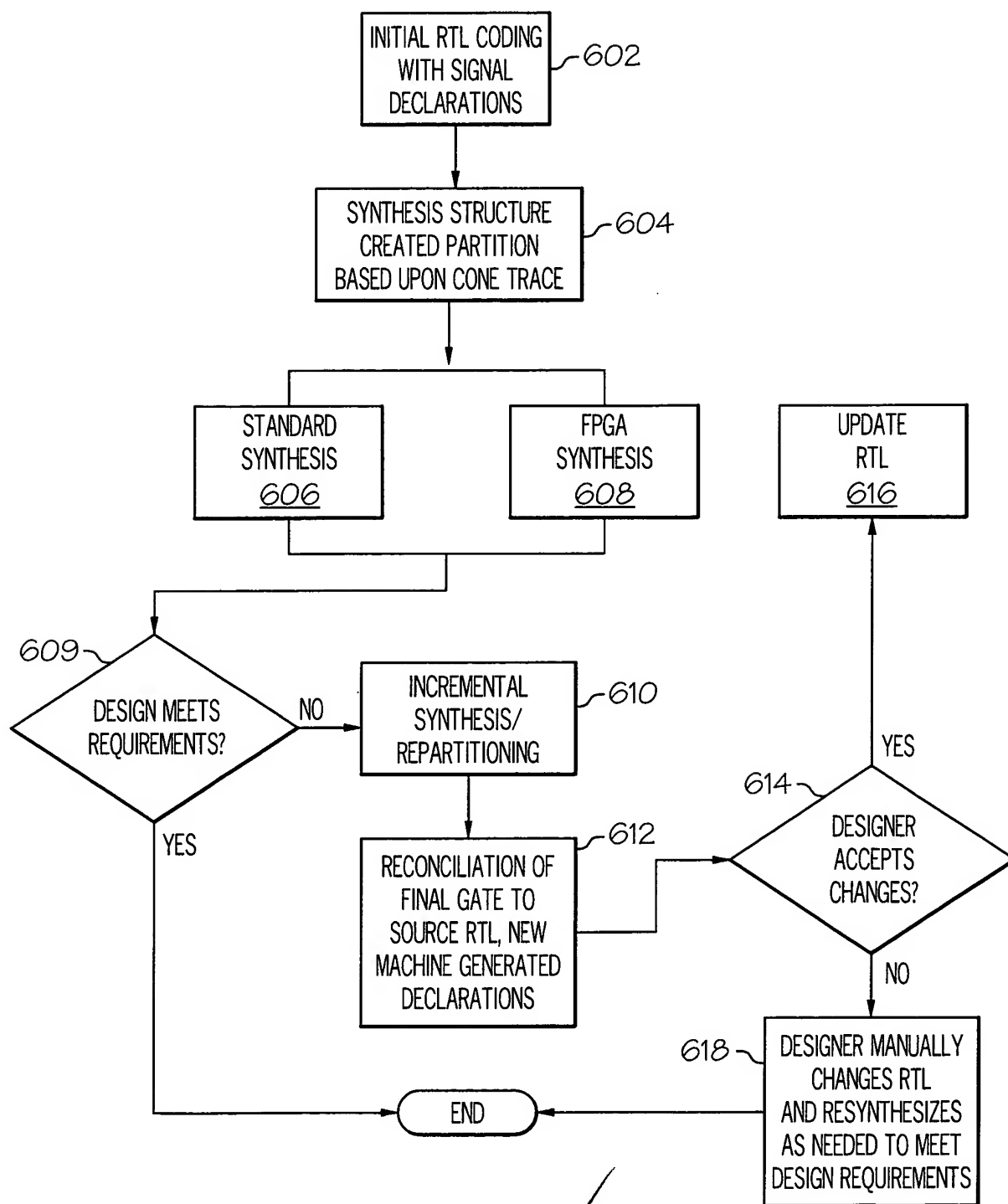


FIG. 6 ✓

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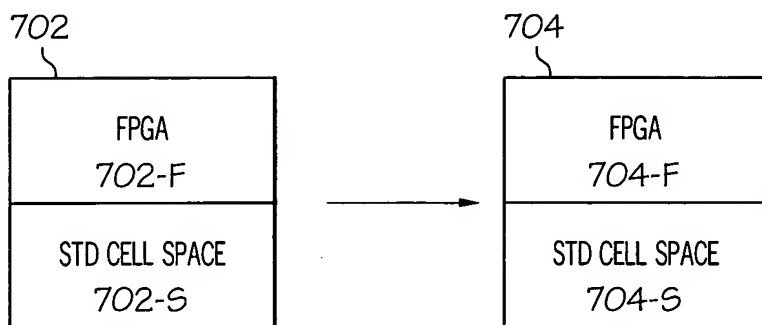


FIG. 7A

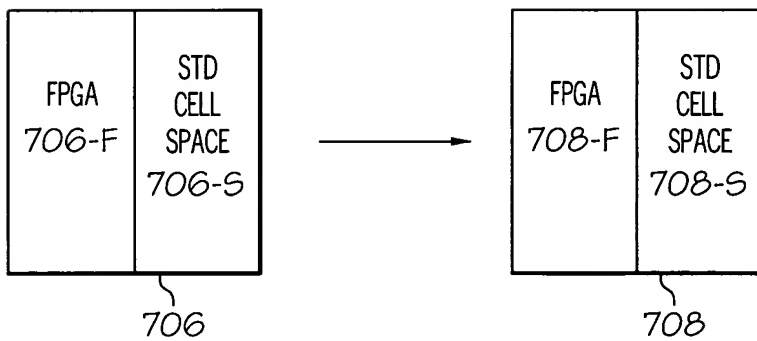


FIG. 7B